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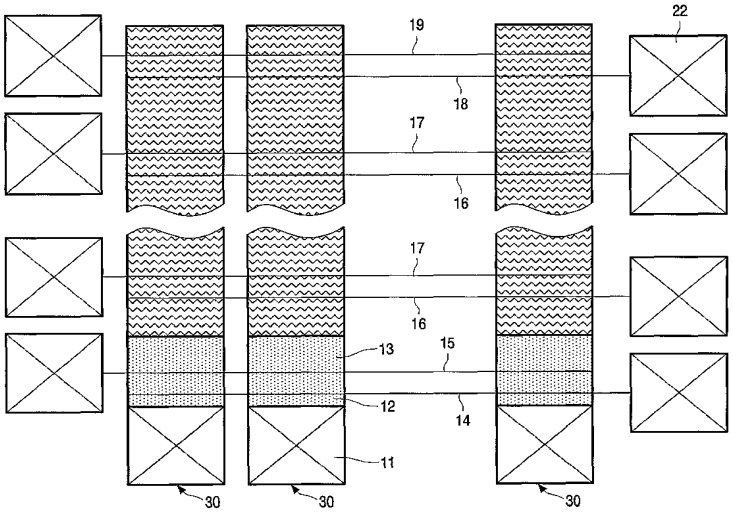
(54) Title: METHOD AND APPARATUS FOR TESTING INTEGRATED CIRCUITS FOR SUSCEPTIBILITY TO LATCH-UP



(57) Abstract: A test module for testing the susceptibility of an integrated circuit design to latch-up, the test module comprising a plurality of test blocks (30), connected in parallel, each test block (30) comprising an injector block (12) for applying a stress current or voltage to the respective test block (30), and a plurality of sensor blocks (13) located at successively increasing distances from the respective injector block (12), each sensor block (13) comprising a PNPN latch-up test structure. The present invention combines the respective advantages of conventional IC stress current testing and latch-up parameter measurement using a standard PNPN latch-up test structure.

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